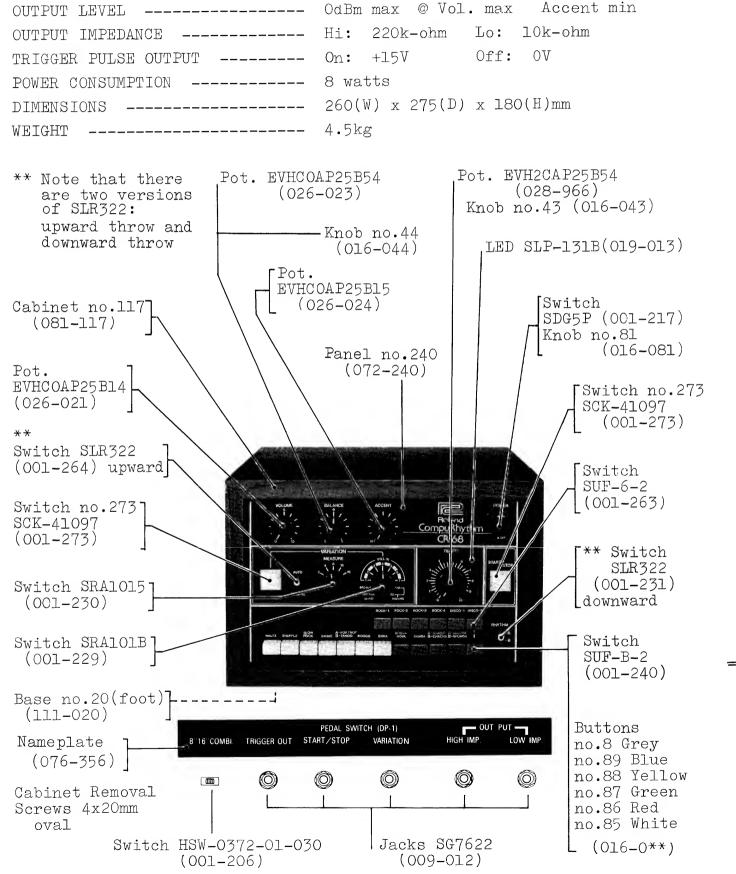
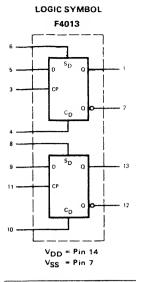
## **CR-68** SERVICE NOTES

## **SPECIFICATIONS**





## CONNECTION DIAGRAM DIP (TOP VIEW)

| ıЦ  | 0,              | V <sub>DD</sub> | 14          |
|-----|-----------------|-----------------|-------------|
| 2 □ | ō <sub>1</sub>  | 02              | 13          |
| 3 □ | CP <sub>1</sub> | ā <sub>2</sub>  | 12          |
| 4 □ | C <sub>D1</sub> | CP₂             | <b>"</b>    |
| 5 🗆 | Dı              | CD2             | <b>1</b> 10 |
| 6 🗆 | S <sub>D1</sub> | D <sub>2</sub>  | D°          |
| 7 🗖 | ٧ss             | S <sub>D2</sub> | <b>]</b> 8  |

NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

#### F4013 TRUTH TABLES

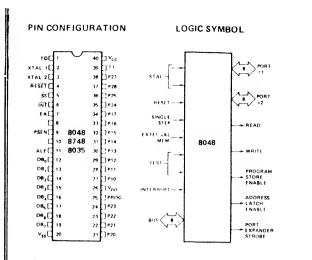
|    | RONOUS<br>UTS | OUT              | PUTS                      |
|----|---------------|------------------|---------------------------|
| CP | D             | Q <sub>n+1</sub> | $\overline{\Omega}_{n+1}$ |
| 7  | L             | L                | Н                         |
| Ţ  | Н             | Н                | L                         |
|    |               |                  |                           |

Conditions: SD = CD = LOW

|                 | RONOUS<br>UTS | ОUТ | PUTS |
|-----------------|---------------|-----|------|
| \$ <sub>D</sub> | CD            | Q   | ā    |
| L               | Н             | L   | Н    |
| Н               | Ł             | Н   | L    |
| Н               | Н             | L   | L    |

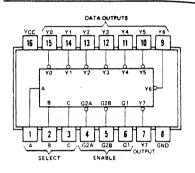
- = I OW Level = HIGH Level
- = Positive-Going Transition
- Don't Care
- On+1 = State After Clock Positive Transition

# F4001 QUAD 2-INPUT NOR GATE LOGIC AND CONNECTION DIAGRAM 14 13 12 11 10 9 8

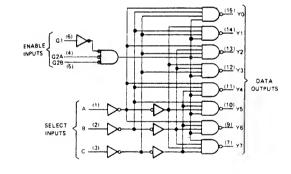


#### **DECODERS/DEMULTIPLEXERS**

SN54LS138, SN54S138 . . . J OR W PACKAGE SN74LS138, SN74S138 . . . J OR N PACKAGE (TOP VIEW)



#### 'LS138 S138

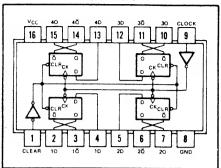


## 'LS138, 'S138 FUNCTION TABLE

|     | INPUTS |   |        |   |    |    | ,  | N IT       | PUT | •  |    |    |
|-----|--------|---|--------|---|----|----|----|------------|-----|----|----|----|
| ENA | ENABLE |   | SELECT |   |    |    |    |            |     |    |    |    |
| G1  | G2*    | С | В      | Α | Y0 | Y1 | Y2 | <b>Y</b> 3 | Y4  | Y5 | Y6 | Y7 |
| Х   | Н      | х | Х      | х | н  | Н  | Н  | Н          | Н   | Н  | Н  | Н  |
| L   | X      | × | X      | X | н  | н  | Н  | н          | Н   | н  | Н  | Н  |
| н   | L      | L | L      | L | L  | Н  | н  | Н          | Н   | н  | Н  | Н  |
| н   | L      | L | L      | н | н  | L  | Н  | Н          | н   | н  | Н  | Н  |
| н   | L      | L | н      | L | н  | Н  | L  | Н          | Н   | Н  | Н  | Н  |
| н   | L      | L | н      | н | н  | н  | Н  | L          | Н   | н  | Н  | Н  |
| н   | L      | н | L      | L | н  | н  | Н  | Н          | L   | н  | Н  | Н  |
| н   | L      | н | L      | н | н  | Н  | Н  | Н          | Н   | L  | Н  | Н  |
| н   | L      | н | н      | L | н  | н  | Н  | Н          | н   | Н  | L  | н  |
| н   | L      | н | н      | н | н  | н  | н  | Н          | н   | Н  | н  | L  |

\*G2 = G2A + G2B

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE



|              | TYPICAL   | TYPICAL       |
|--------------|-----------|---------------|
| TYPES        | MAXIMUM   | POWER         |
| ITPES        | CLOCK     | DISSIPATION   |
|              | FREQUENCY | PER FLIP-FLOP |
| 174, 175     | 35 MHz    | 38 mW         |
| 'LS174 LS175 | 40 MHz    | 14 mW         |
| 'S174 'S175  | 110 MHz   | 75 mW         |

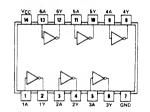
#### QUADRUPLE D.TYPE FLIP-FLOPS

## FUNCTION TABLE

| (EACH FLIP-FLOP) |          |   |            |                  |  |  |  |  |
|------------------|----------|---|------------|------------------|--|--|--|--|
|                  | INPUTS   |   |            |                  |  |  |  |  |
| CLEAR            | CLOCK    | D | Q          | ãt               |  |  |  |  |
| L                | х        | X | L          | н                |  |  |  |  |
| н                | <b>†</b> | н | н          | L                |  |  |  |  |
| н                | †        | L | L          | н                |  |  |  |  |
| н                | L        | x | $\alpha_0$ | $\bar{\alpha}_0$ |  |  |  |  |

- H = high level (steady state)
- L = low level (steady state)
- 1 = transition from low to high level Q<sub>0</sub> = the level of Q before the indicated steady-state
- input conditions were established.
- † = '175, 'LS175, and 'S175 only

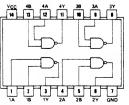
#### HEX INVERTERS



SN5404 (J) SN54H04 (J) SN54LS04 (J W)

SN74H04 (J N SN74L04 (J N) SN54S04 (J W) SN74S04 (J N)

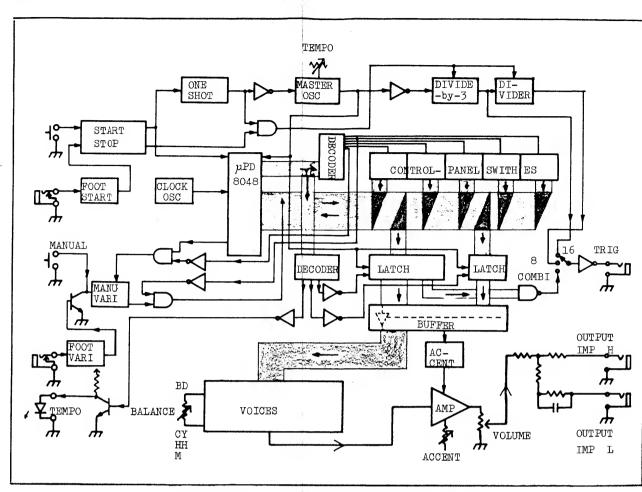
#### QUADRUPLE 2-INPUT POSITIVE-NAND GATES



SN54H00 (J) SN54L00 (J)

SN54S00 (J. W)

SN74H00 (LLN) SN74L00 (J N) SN54LS00 (J W) SN74LS00 (J N)



## **CIRCUIT DESCRIPTION**

COMPUTER BOARD GL-10

The uPD8048 is an 8-bit parallel computer fabricated on a single sillicon chip. The 8048 contains a lk  $\times$  8 ROM program memory, a 64  $\times$  8 RAM memory, 27 I/O lines, an 8-bit timer/counter and clock circuits.

Used on this board is a uPD8048C-015 version in which program and data dedicated to the CR-68 are stored in the program memory.

#### 1. SCANNING for IDENTIFYING PANEL SWITCH SETTINGS

The uPD8048 reads panel switch settings by scanning the lines through Port 2 (P24-P27) of IC10, IC8 (74LS-138, Decoder) and Port 1 (P10-P17) of IC10. The output from IC8 (Binary-to-octal decoder) goes—through one of properly arranged switches and matrix to port 1. For example let's assume that SWING switch is—depressed. When A input of IC8 is high and B, C and G2B inputs—are low as shown in Fig. 1. The output of 1 goes low and other outputs go high.

Since Port 1 (P10-P17) functions now as an input port and 1 of IC8 is low with SWING switch on, only P10 of IC10 goes low. IC10 reads this condition of Port 1 and identifies that SWING switch is depressed. By repeating such scanning, the computer can identify every switch setting in sequence.

This scanning and reading, in STOP mode, are performed continously in very short periods by pulses with durations of several microsecons, bur after START switch is pressed, this scanning is performed once a measure—just before the measure is initiated.

#### 2. SENDING OUT RHYTHM PATTERNS

After panel settings are identified as described above, the data corresponding to the identification is selected from contains of the ROM and fed into Fort 1 and Port 2.

Tow 74LS138's (IC8 and IC9) are used in parallel to constitute a binary-to-hexadecimal decoder. In this case, Port 1 of IC10 functions as an output port.

#### 3. VARIATION TURNED ON WITH MANUAL BUTTON

Since the computer reads data once in one measure, if MANUAL button is pressed during the period between one reading and another, a circuit is required to memorize the switching, which consists of IC4 (74LSOO) and other components.

IC4a and IC4b constitute an RS flip-flop which is reset when START/STOP button is tapped to start the rhythm unit. When reset in this way, pin 3 of IC4a goes high, and pin 6 of IC4b goes low and hereafter this condition is held.

In reading, with MANUAL button off, pin 6 of IC4b remains low and pin 8 of IC4c is held high independent of the condition of pin 10 of IC4c. When MANUAL button is pressed, pin 5 of IC4b immediately goes low and RS flip-flop is set. Pin 3 of IC4a goes low and pin 6 of IC4b goes high and this condition is held.

When a negative going pulse is sent out from 4 of IC8 while reading switch positions, the pulse is inverted by IC2c and this inverted positive pulse is fed to pin 10 of IC4c. Since pin 9 of IC4c is kept high, a negative going pulse is sent out from pin 8 of IC4c and fed into Port 1 through D209. Thus, the computer detects that MANUAL button has been pressed.

Immediately after reading, the computer sends out a negative going pulse from 0 of IC8 to reset RS flip-flop. To prevent malfunction, this pulse (after invertion by IC2a) and a pulse from ALE of IC10 are NANDed to produce a reset pulse. see Fig. 2

#### 4. CLOCK GENERATOR IC3e. IC3f

This circuit, a clock generator from which pulses are emitted to synchronize the operations carried out by the computer, is a CR oscillator consisting of IC3e, IC3f and other components. The oscillator generates clock signals of about 3MHz which are fed to XTAL pin of IC10.

#### 5. MASTER OSCILLATOR Q101, Q102

This oscillator determines the tempo of the rythm and is a multivibrator consisting of Q101, Q102 and other components, whose oscillation period is variable from 10ms - 200ms with TEMPO control VR2.

#### 6. START CIRCUIT IC5b, ICla - ICld, IC2b

This circuit consists of IC5b (D flip-flop) and other components. The output "Q" on pin 1 of IC5b is connected to Tl of IC10.

Immediately after POWER switch is set to ON a short positive going pulse with the time constant of R212 and C208 is generated at pin 11 of ICld and resets IC5b. Q on pin 1 goes low and  $\overline{\rm Q}$  on pin 2 goes high. Consequently, when POWER switch is set to ON, IClO is always set in the idling mode. (When T1 of IClO is low, the computer stops all functions except scanning). When START button is pressed, a positive pulse is generated at pin 4 of IClb which is fed into pin 3 of

IC5b. Q goes high and  $\overline{Q}$  goes low. Then T1 of IC10 goes high to start the rhythm unit.

The one shot pulse generator consisting of ICla, IClc, IClb and other components detects the leading edge of an output waveform from Q on pin 1 of IC5b and generates a pulse with a duration of about 30ms which resets the master oscillator when the rhythm unit starts.

See Fig. 3

#### 7. FOOT SWITCH CIRCUIT IC3a - IC3d

The foot switch circuit for START/STOP consisting of IC3a, IC3b and other components, and that for VARIA-TION consisting of IC3c, IC3d and other components, are almost the same circuit. A CR time constant circuit combined with a schmitt trigger circuit is used to prevent malfunction caused by foot switch chattering.

8. DIVIDER IC7a, IC5a, IC6a, IC6b

To send out clock pulses with 8 beat and 16 beat to TRIGGER OUT jack, a circuit is required to divide the output signals from the master oscillator into 1/3 and 1/6. The circuit consists of four MC14013B's (D flip-flop, IC7a, IC5a, IC6a, and IC6b) and other components. IC7a, used as an inverter, shapes output waveforms from the master oscillator to prevent the divide-by-3 circuit from malfunctioning. The singals are fed into the divide-by-3 circuit consisting of IC5a and IC6b to be converted to signals with 16 beat and sent from Q on pin 1 of IC6b.

Signals fed from  $\overline{\mathbb{Q}}$  on pin 2 of IC6b to CP on pin 11 of IC6a are divided again to be converted to signals with 8 beat and sent out from  $\mathbb{Q}$  on pin 13 of IC6a. see Fig.4

#### VOICING BOARD VG-12

#### 1. LATCH IC1 -- IC3

This circuit, consisting of three 74LS175 flip-flops, take output pulses to be latched from Port 1 and Port 2 through IC2d and IC2e (clock), and take pulses from the master oscillator to clear the preceding latch, producing 5V positive going pulse, i.e. rhythm pattern, with the same duration as output pulse of the master oscillator.

The output pulses from the flip-flops are converted by Q25-Q35 into negative going pulses with a +15V-OV swing and fed into inputs of the voicing circuits. see Fig. 5

#### 2. ACCENT CIRCUIT Q21. Q24. VR14

This circuit is used to add accent to a rhythm according to a preset accent pattern by changing the sound level at the output amplifier. The circuit consists of the ACCENT (VR14), Q21, Q24 and other components. An accent pulse from  $\overline{Q}$  on pin 3 of IC1 passes through Q21 and then is differentiated and integrated to be converted to a proper envelope signal which is fed into the gate of FET (Q24).

Q24 is off when a signal is not provided at the gate. In this case, the voltage of the output signal from Q9 is divided by the ratio of R137 (68k-ohm) to the input impedance of Q10 and is fed into Q10. When a signal is fed into the gate, Q24 is turned on.

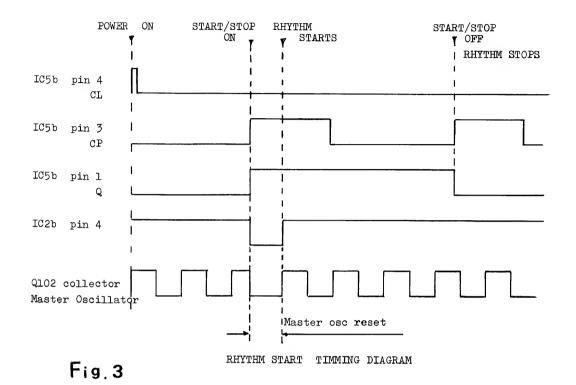
With ACCENT control at 10, most the signal flows into the accent potentiometer and Q24, but very little into R137, giving a high level output signal which is used to add accent.

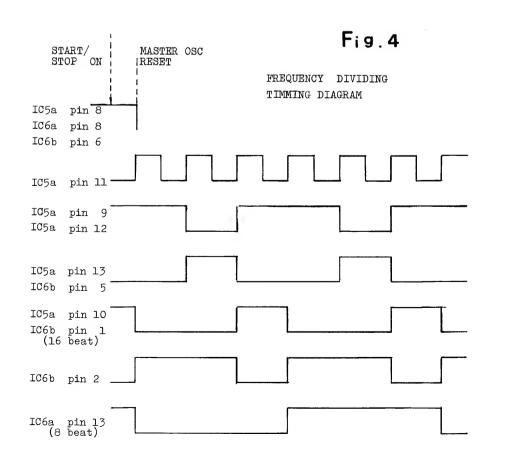
#### 3. LEAKAGE SOUND KILLER Q20, Q23

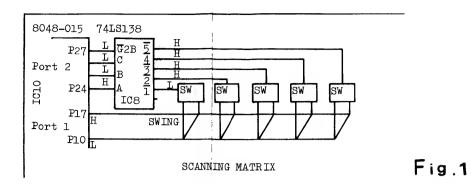
These circuits are designed to kill sound from the voicing circuits generated by transient voltage when power is turned on or off. When power is on, Q20 will not function normally until C79 charges enough in respect to the emitter.

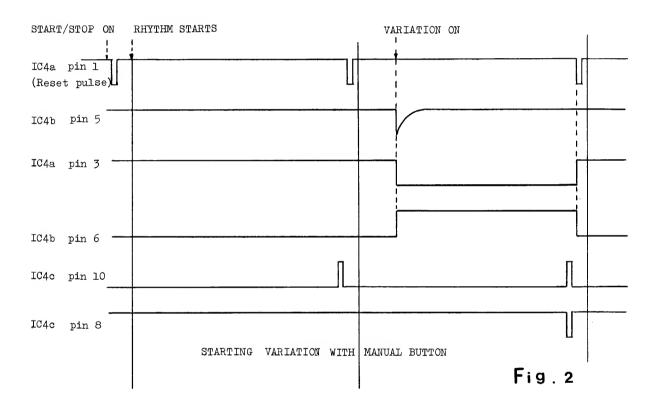
The voltage drop at the gate of Q23 is quicker than it is at the drain or source after trun, so that Q23 is shut off.

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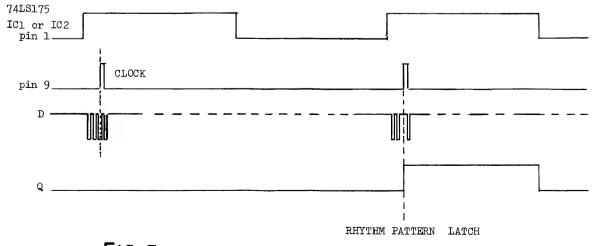


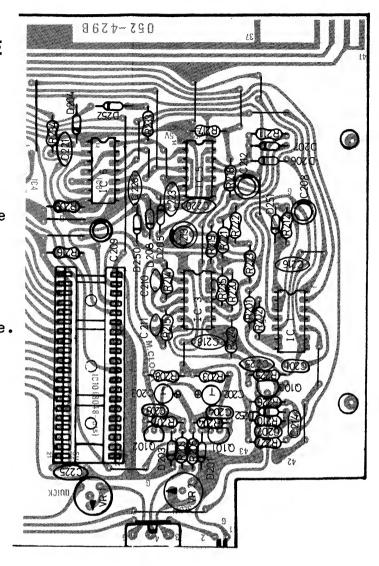
Fig.5

Refer to the function table on page 1

## GL-10B(142-010B) VIEW from FOIL SIDE Serial No.822000 and up

Portions of pattern not shown remain unchanged.

Both GL-10A and GL-10B correspond to the same circuit diagram since some components are attached on the foil side or connected in series in the form of pyramid on GL-10A and accommodated on GL-10B in place.

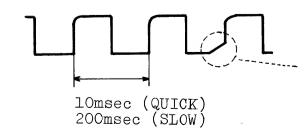


<u>CAUTION</u>: Always handle MOS ICs while wearing an earth grounded wristband to prevent failure of ICs due to electrostatic discharge. All test equipment must also be earth grounded.

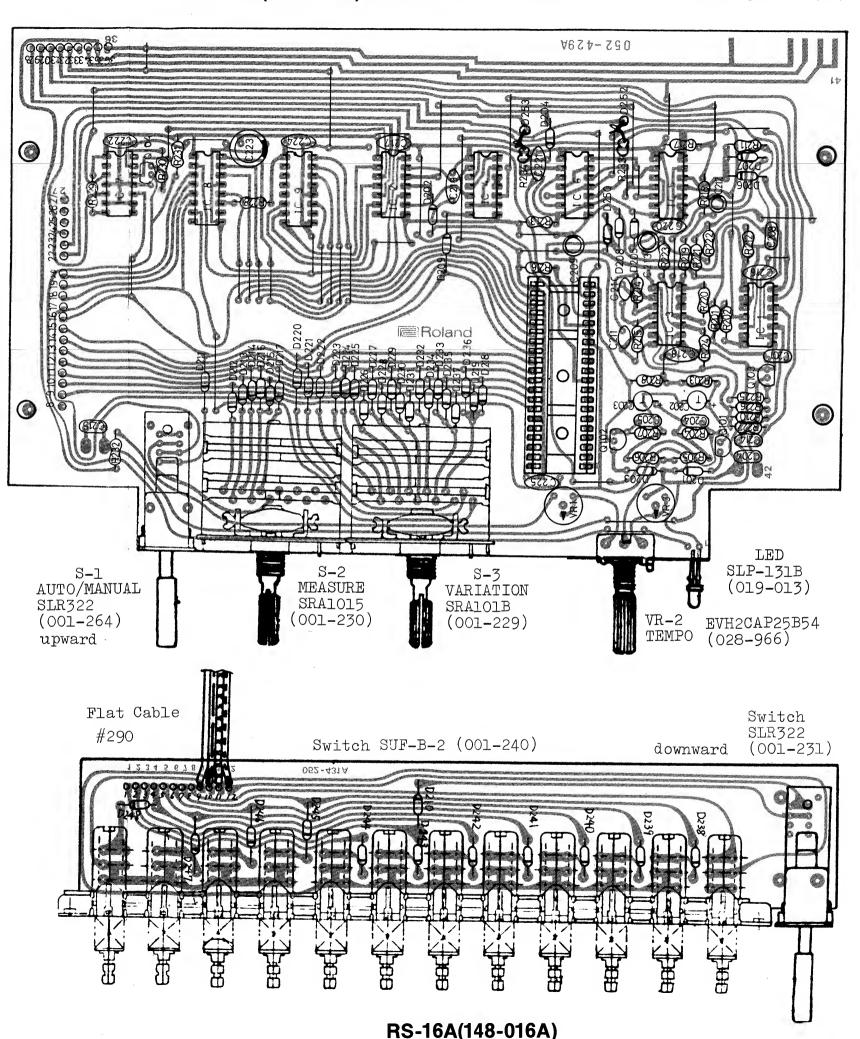
#### RHYTHM TEMPO ADJUSTMENT

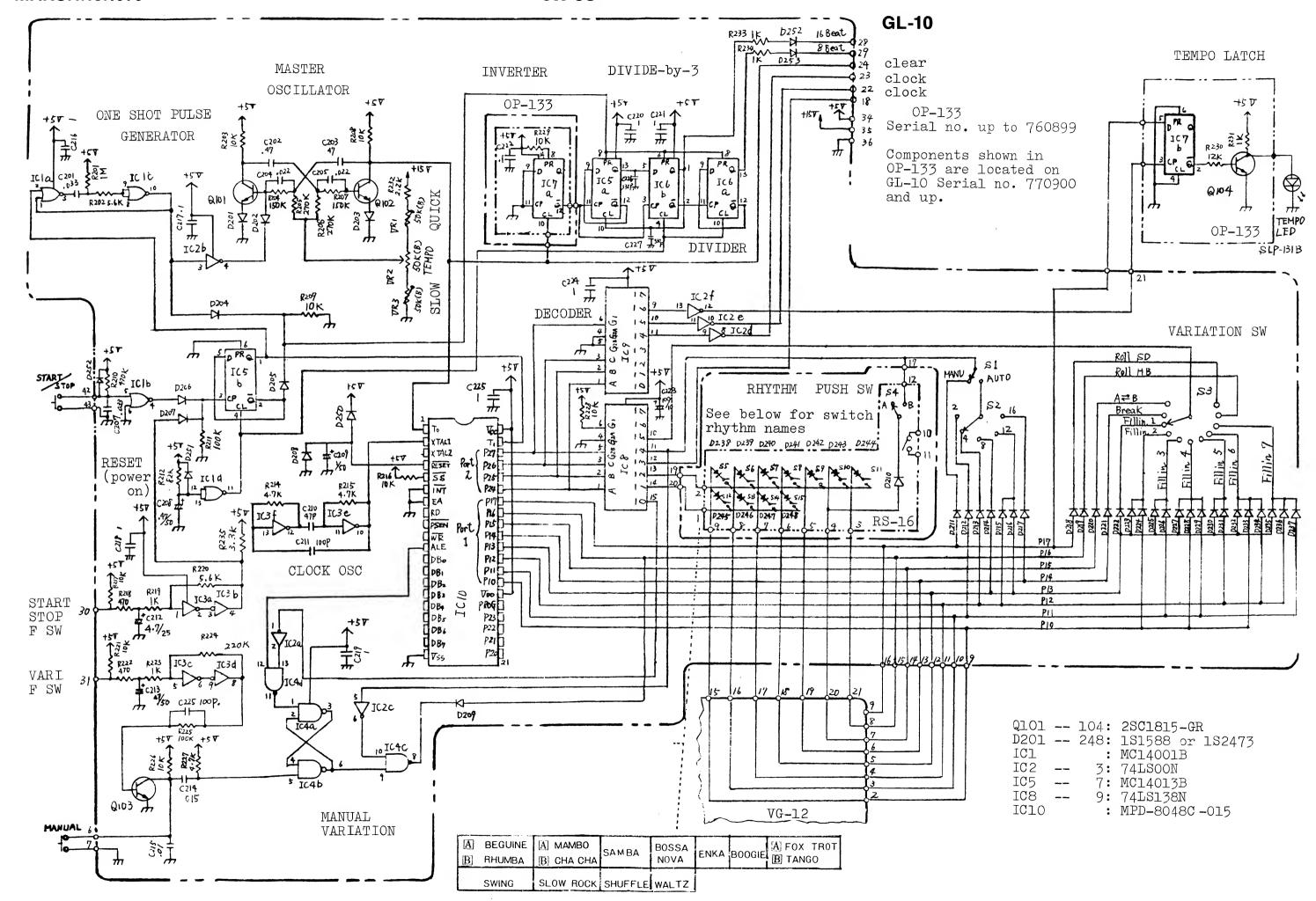
- Connect scope to Q102 collector (Master Oscillator).
   Turn TEMPO knob full clockwise (QUICK).
- Adjust VRl for 10ms between fall or rise of squares.
- 3. Turn TEMPO knob full counterclockwise (SLOW).

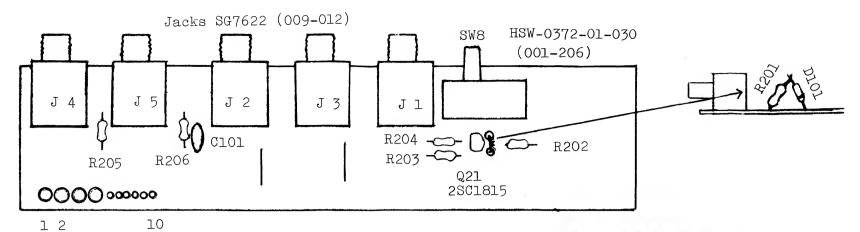
  Turn VR3 in the direction in which the period becomes shorter than 200ms. Stop, then rotate VR3 slowly in the reverse direction until the period is 200ms.
- 4. Repeat steps 3 and 4.



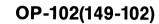
If bottom portion is insuficiently saturated, replece Q101 and Q102 with a new pair of the same rank.

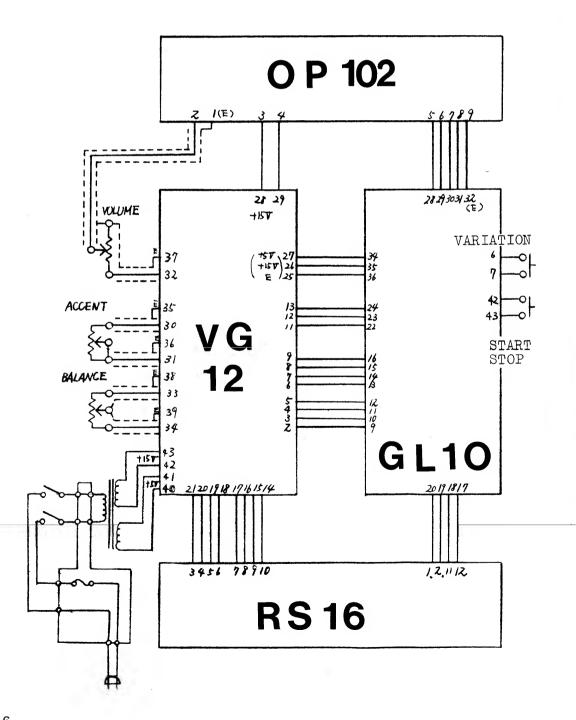


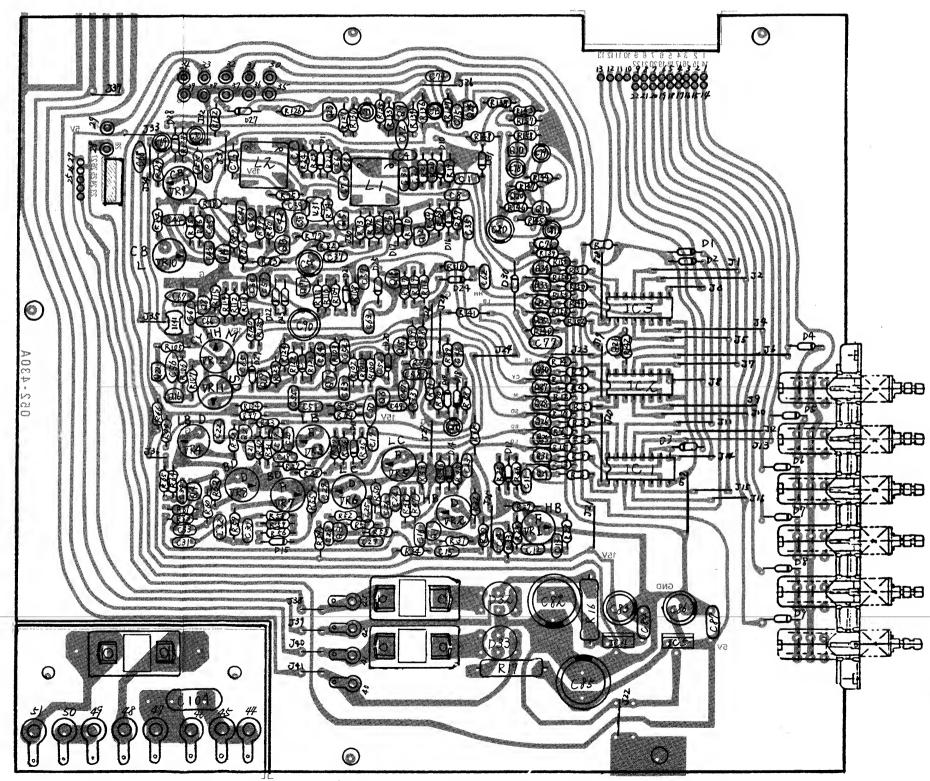


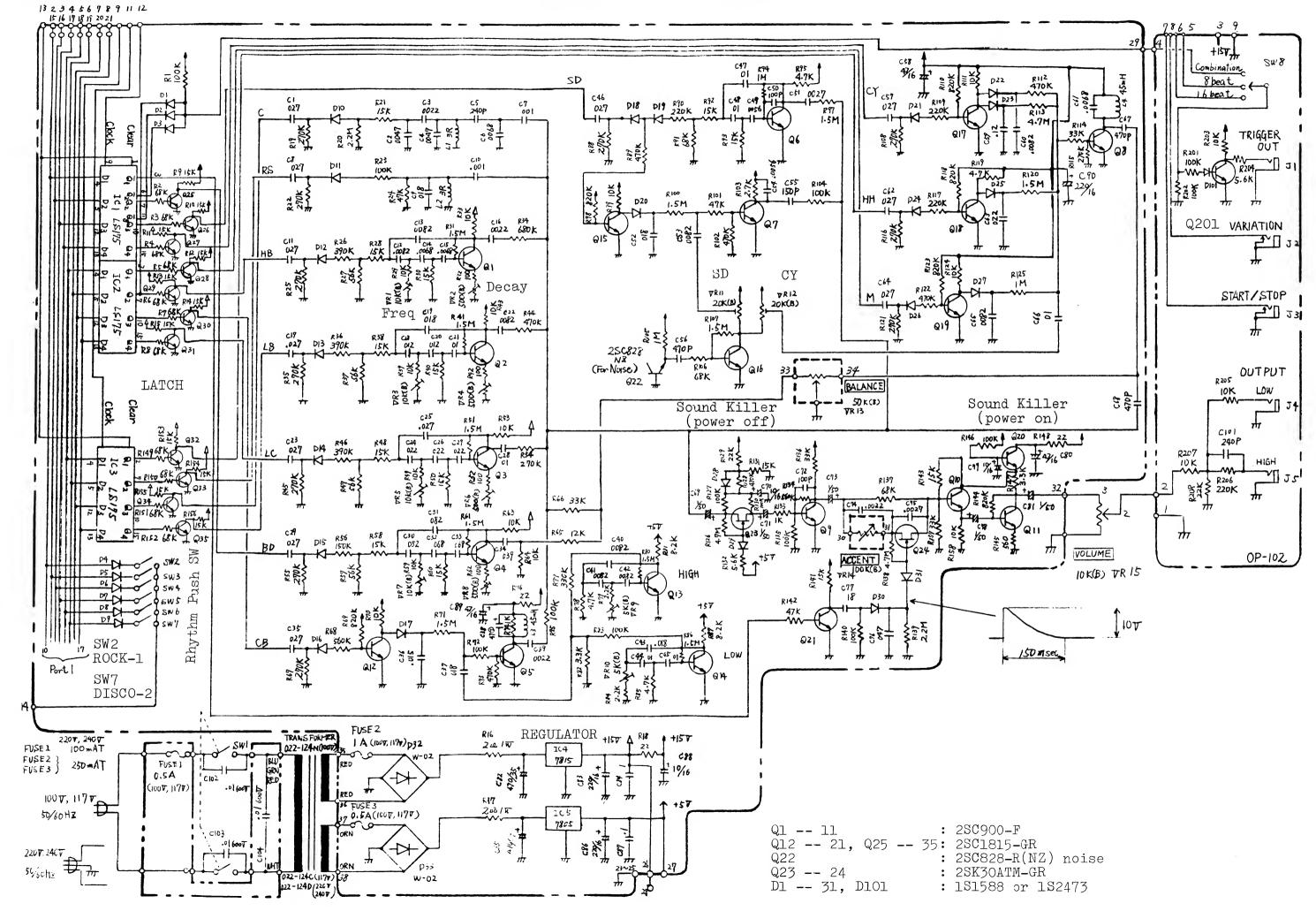


VG-12A(143-012A)









#### RHYTHM PATTERNS







SLOW ROCK











BOSSA NOVA







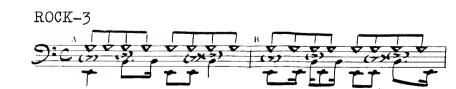


ROCK-1



ROCK-2





ROCK-4

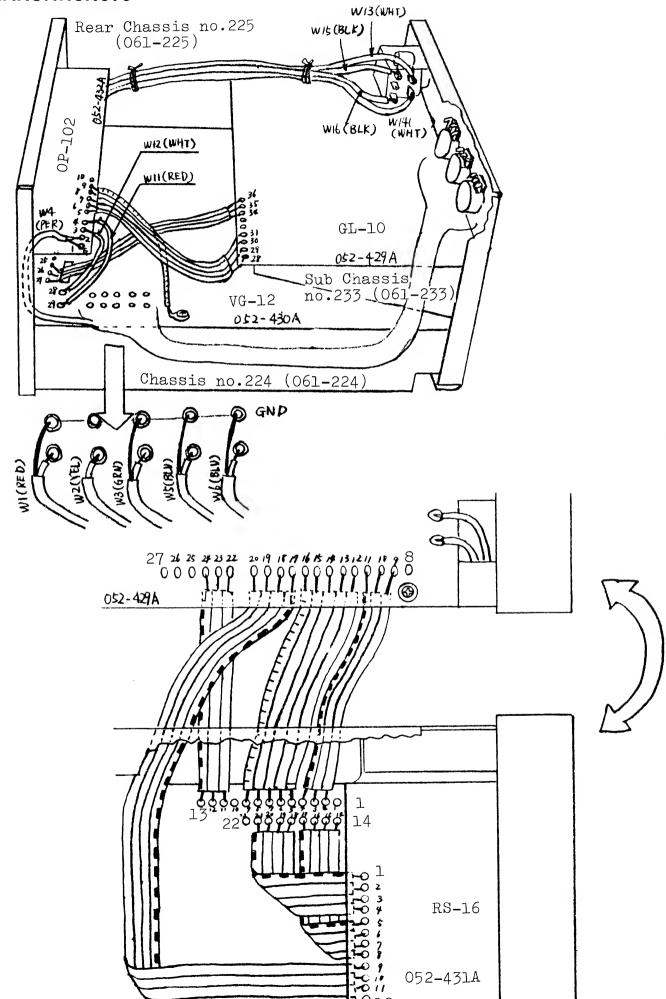




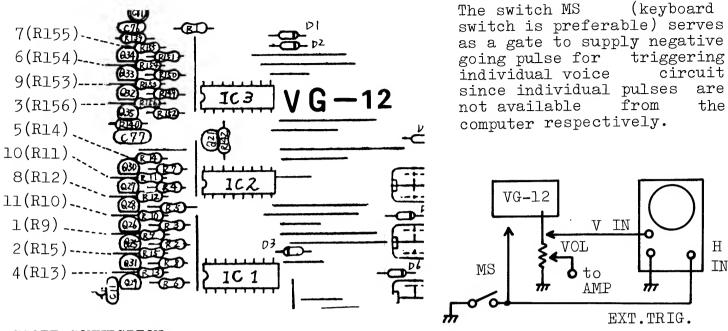




### MARCH.15.1979



## **CHECK & ADJUSTMENT**



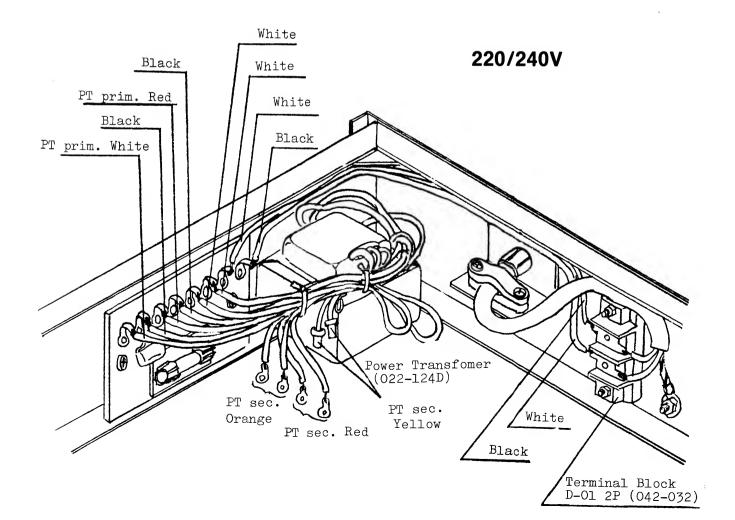
SCOPE CONNECTION

1 through ll: as illustrated

Q13, Q14: V IN -- to collector. H -- Internal TRIG with proper time base.

| VOICE  | Ccn-                | FF  | REQUENC  | Y        | DECAY   | DECAY TIME |         | TUDE                              | set                |  |
|--|---------------------|---|----------|----------|---------|------------|---------|-----------------------------------|--------------------|--|
| to be adjusted                                       | nect<br>scope<br>to | Adjust                                    | fo<br>ms | or<br>Hz | Adjust  | for<br>ms  | Adjust  | for<br>V-pp                       | BALANCE<br>at      |  |
| BASS DRUM  | 1                   | VR7                                       | 16       | 62.5     | VR8     | 100        | *       | 1.4                               |                    |  |
| LOW CONGA  | 2                   | VR5                                       | 4.8      | 208      | VR6     | 100        | *       | 1.4                               | full-<br>counter-  |  |
| LOW BONGO  | 3                   | VR3                                       | 2.5      | 400      | VR4     | 40         | *       | 0.6                               | clockwise          |  |
| HIGH BONGO   | 4                   | VRl                                       | 1.66     | 600      | VR2     | 40         | *       | 0.7                               |                    |  |
| COW BELL H   | Q13 C               | VR9                                       | 1.25     | 800      | shift s | cope V     | IN_from | m                                 |                    |  |
| COW BELL L   | Q14 C               | VR10                                      | 1.8      | 555      | YOLUME, | H TN       | to Inte |                                   | '' <del>X</del> '' |  |
| COW BELL   | 5                   | restore scope con-<br>nection to previous |          | *        | 60      | *          |         | non-<br>adjustable:<br>just check |                    |  |
| RIM SHOT   | 6                   | C9  | 0.676    | 1,480    | *       | 5          | *       | 4.4                               | J 420 0 110 0 11   |  |
| CLAVES   | 7                   | C4  | 0.38     | 2,630    | *       | 18         | *       | 0.7                               |                    |  |
| MARACAS  | 8                   | adjust                                    | ing VRl  | 2 on     | *       | 18         | VR12    | 1.5                               |                    |  |
| HI-HAT   | 9                   | any on                                    | e voice  | makes    | *       | 50         | VR12    | 1.5                               |                    |  |
| CYMBAL   | 10                  | all                                       |          |          | ×       | 250        | VR12    | 1.5                               | full-<br>clockwise |  |
| SNARE DRUM   | 11                  |   |          |          | *       | 60_        | VRll.   | 1.0                               |                    |  |
| 1.5V 1V pp 20msec after sound initiation; SNARE only |                     |   |          |          | AMPLITU |            | DECAY T | IME                               |                    |  |

Figures in the table show factory standard and may be slightly deviated for personal taste or to meet frequency response of an amlifier being used.



| Nobs Push Buttons  | 081-117<br>111-020<br>072-240<br>076-356<br>061-224<br>061-233            | Base no.20 (foot) Panel no.240 Nameplate no.356 rear above jacks Chassis no.224 main Chassis no.233 sub GL-10 mounting | SWITCHES  OO1-180 SDG-5P power OO1-273 SCK-41097 keyboard OO1-206 HSW-0372-01-030 slide TRIG OUT OO1-230 SRA1015 rotary MEASURE OO1-229 SRA101B rotary FILL IN OO1-263 SUF-6-2 push gang ROCKDISCO-2 OO1-240 SUF-B-2 phsh gang WALTZ OO1-231*SLR322 lever RHYTHM A/B OO1-264*SLR322 lever AUTO/MANUAL |
|--|---|--|---|
| 016-044 no.44 rotary   |   | KNOBS PUSH BUTTONS   | *oposite throw directions   |
| 016-088  | 016-044<br>016-081<br>016-008<br>016-085<br>016-086                       | no.44 rotary no.81 blk power switch Button no.8 gray no.85 white no.86 red   | 026-023 EVHCOAP25B54 50kB BALANCE<br>026-024 EVHCOAP25B15 100kB ACCENT<br>026-021 EVHCOAP25B14 10kB VOLUME<br>028-996 EVH2CAP25B54 50kB TEMPO PC  |
| O22-030  | 016-088   | no.88 yellow<br>no.89 blue   | 028-001 EVTR4A00(SR19) 500-ohm<br>028-003 E <b>V</b> TR4A00(SR19) 5k<br>028-004 EVTR4A00(SR19) 10k  |
| 022-033  | 022_030   |  | 028-005 EVTR4A00(SR19) 20k<br>028-006 EVTR4A00(SR19) 50k  |
| 148-016A RS-16A etch mask 052-431A 142-010A GL-10A etch mask 052-429A 143-012A VG-12A etch mask 052-430A 149-102 OP-102 etch mask 052-432  ICS  020-141 74LS175N or CMOS40175 020-106 7805UC regulator +5V 020-138 74LS138N 020-124 74LS04N 020-120 74LS04N 020-120 74LS04N 020-120 MC14001BCP 020-041 MC14013BCP 020-041 MC14013BCP 179-022 MPD-8048C-15  TRANSISTORS  017-06 2SC1815-GR 017-016 2SC3828-R NZ selected for noise 017-016 2SK30A-GR FET  DIODES  018-059 1S1588 018-082 W-02 bridge 1.5A   | 022-033<br>022-124N<br>022-1240   | Coil no.33 3R 700mH<br>FPT no.124N 100V<br>FPT no.124C 117V  | CAPACITORS<br>032-095 0.47uF 35V K tant.  |
| 142-010A GL-10A etch mask 052-429A 143-012A VG-12A etch mask 052-430A 149-102 OP-102 etch mask 052-430A 149-102 OP-102 etch mask 052-432  OR-026 CEE 100mAT prim 220/240V 08-056 CEE 100mAT sec 220/240V  ICS MISCELLANEOUS  020-141 74LS175N or CMOS40175 020-108 7805UC regulator +5V 020-108 7815UC regulator +5V 020-118 74LS138N 020-124 74LS04N 020-124 74LS04N 020-127 74LS04N 020-129 MC14001BCP 020-041 MC14013BCP 179-022 MPD-8048C-15  TRANSISTORS  017-106 2SC1815-GR 017-016 2SC328-R NZ selected for noise 017-016 2SK30A-GR FET  DIODES  018-059 1S1588 018-082 W-02 bridge 1.5A  |   | PCBs   | FUSES   |
| 020-141 74LS175N or CMOS40175 020-106 7805UC regulator +5V 020-108 7815UC regulator +15V 020-138 74LS138N 020-124 74LS04N 020-120 74LS00N 020-169 MC14001BCP 020-041 MC14013BCP 179-022 MPD-8048C-15 017-016 2SC1815-GR 017-016 2SC828-R NZ selected for noise 017-016 2SK30A-GR FET  DIODES  012-003 Fuse Clip TF-758 012-040 IC Socket ICC30-040-350G 40 pin 009-012 Jack SG7622 064-134 Holder no.134 line cord 047-003 Line Cord Clamp 1702B 120-001 Long Nut no.1 3x10mm stand-off 047-023 Line Cord Clamp 1702B 047-023 Line Cord Clamp 1702B 053-289 Flat Cable no.289 5 pin 053-290 Flat Cable no.290 4 pin  * Resistors, mylars and ordinary electrolytic capacitors are omitted. selectrolytic capacitors are omitted.   | 142-010A<br>143-012A  | GL-10A etch mask 052-429A<br>VG-12A etch mask 052-430A   | 008-056 CEE 100mAT prim 220/240V  |
| 020-106 7805UC regulator +5V 020-108 7815UC regulator +15V 020-138 74LS138N 020-124 74LS04N 020-120 74LS00N 020-169 MC14001BCP 179-022 MPD-8048C-15 053-290 Flat Cable no.290 4 pin 053-290 Fl |   | ICs  | MISCELLANEOUS   |
| TRANSISTORS  017-106  2SC1815-GR  017-021  2SC900-F  | 020-106<br>020-108<br>020-138<br>020-124<br>020-120<br>020-169<br>020-041 | 7805UC regulator +5V<br>7815UC regulator +15V<br>74LS138N<br>74LS04N<br>74LS00N<br>MC14001BCP<br>MC14013BCP            | 012-040 IC Socket ICC30-040-350G 40 pin<br>009-012 Jack SG7622<br>064-134 Holder no.134 line cord<br>047-003 Line Cord Strain Relief<br>047-023 Line Cord Clamp 1702B<br>120-001 Long Nut no.1 3x10mm stand-off<br>053-289 Flat Cable no.289 5 pin  |
| 017-106 2SC1815-GR 017-021 2SC900-F  | 179-022   | MPD-8048C-15   | 055-290 flat Cable no.290 4 pin   |
| 018-059 1S1588<br>018-082 W-02 bridge 1.5A   | 017-021<br>017-046  | 2SC1815-GR<br>2SC900-F<br>2SC828-R NZ<br>selected for noise  |   |
| 018-082 W-02 bridge 1.5A   |   | DIODES   |   |
|  | 018-082   | W-02 bridge 1.5A   |   |